REMARKS

Claims 1-23 are pending this application of which claims 1 and 18 are the independent claims. Favorable reconsideration and further examination are respectfully requested.

Claims 1-3, 5-9, 12, 13, and 17-19 were rejected under 35 U.S.C. §102(b) as being anticipated by Panchou et al. Applicants have amended claim 1 to define the invention more clearly. Applicants respectfully traverse the rejection of claim 18.

Claim 1 defines a semiconductor structure having a semiconductor substrate and a compliant interconnect element disposed on a first surface of the substrate. The compliant interconnect element defines a chamber between the first surface of the substrate and the interconnect element.

Claim 18 defines a method for forming a semiconductor structure. The method includes providing a semiconductor substrate and providing a compliant interconnect element on a first surface of the substrate. The compliant interconnect element defines a chamber between the compliant interconnect element and the first surface of the substrate.

Panchou does not disclose or suggest having a chamber between the first surface of the substrate and the compliant interconnect element, as recited in claims 1 and 18. Rather, Panchou has vias that are through the compliant interconnect element. Thus, these vias are not between the first surface of the substrate and the compliant interconnect element.

Furthermore, Panchou does not teach or describe a compliant interconnect element defining "a chamber" as recited in claims 1 and 18. Panchou shows vias that go through a compliant interconnect element, but none that define a chamber. Panchou does not describe an enclosed space or cavity that constitutes a chamber. Rather, these vias are described in Panchou as merely holes, not chambers.

For at least the foregoing reasons, claims 1 and 18 are believed to be allowable.

The remaining claims depend either from claim 1 or claim 18. These claim therefore are also believed to be allowable.

In view of the foregoing remarks, the entire application is believed to be in condition for allowance and such action is respectfully requested at the Examiner's earliest convenience.

All correspondence should be directed to the undersigned at the address shown below. Applicants' undersigned attorney can be reached by telephone at the number shown below.

No fee is believed to be due for this Amendment; however, if any fees are due, please apply such fees to Deposit Account No. 06-1050 referencing Attorney Docket 13292-007001.

Respectfully submitted,

Date: December 23, 2002

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

--1. (Once Amended) A semiconductor structure, comprising:

a semiconductor substrate; and

a compliant interconnect element disposed on a first surface of the substrate, said compliant interconnect element defining a chamber between the first surface of the substrate and [a surface of] the interconnect element.--